Optimum Bias Point for AC Coupled Source Follower

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Problem: In many circuits a high input impedance voltage follower is needed. Op-amps are good at this task but can be expensive. On the other hand, the N-FET source follower shown in figure 1 can be produced at a very low cost. This low cost circuit also has amazing performance. Signal transfer of this topology to the V_s terminal is well documented and may also be called "common drain" (because the drain is held a AC ground). What isn't well documented is what happens to this circuit when the output is AC coupled to a load resistor R_L as shown here in figure 1:

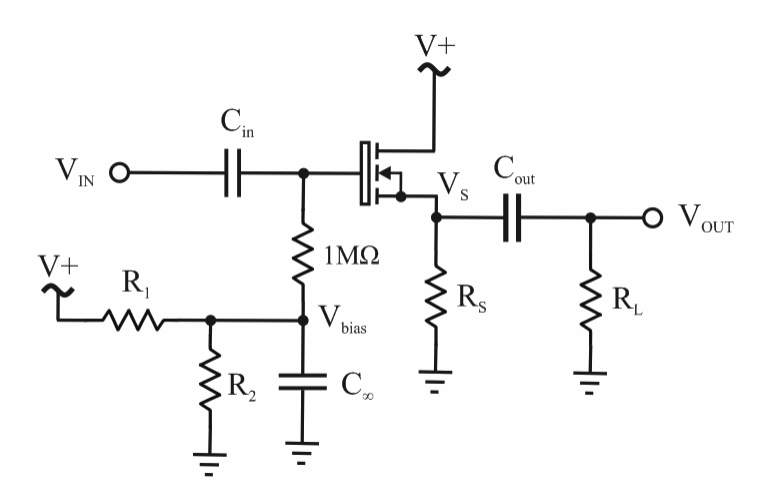

Figure 1 – FET Source Follower with AC coupled output load

FET Follower Feature	Value
Current Gain	∞
Voltage Gain	~ 1
Input Impedance	∞
Output Impedance	$R_S \parallel (1/g_{fs})$

Table 1. – FET Follower Features

The features of the source follower are fabulous:

Input Impedance:. The AC input impedance of this circuit is limited mostly by the gate capacitance of the FET that is used. For the circuit shown in figure 1 the input impedance will be 1 MΩ in parallel with the FETs input capacitance which can be as small as a few pico-Farads for a carefully selected FET. The actual DC impedance

looking directly into the FET's gate is so high it is often not shown on the FET datasheet but can be expected to be on the order of 10^9 Ohms or more.

Output Impedance: Note also that the output impedance at the source is very low. At first glance it appears to be R_S but it is actually $R_S \parallel (1/g_{fs})$ where g_{fs} is the forward transconductance of the FET. For a typical general purpose FET like BSS138 g_{fs} is 0.5 siemens. This means the output impedance at the source is on the order of 2 Ohms—very nice indeed.

These features are all well documented and, as long as the output is DC coupled, the operation of the source follower circuit is trouble free. But what happens when an output load is AC coupled to this circuit as shown in figure 1? This is where subtle trouble can creep into the design.

When output load R_L is AC coupled, the small signal output impedance of the circuit remains as shown in table 1, however, the FET's source is no longer be able to pull the output all the way to ground (see figure 2). Further, when the FET is in this fully off region, the stage output impedance is no longer $R_S \parallel (1/g_{fs})$ but instead becomes R_S–a much higher value.

If this situation is fully understood then it should be possible to bias the FET optimally for maximum output voltage swing. To do this, start by selecting a desired value for $V_{p\text{-}p,max}$ that is less than V+. The circuit cannot swing the full amount unless R_L is infinite or there is infinite bias current, so select a reasonable value for $V_{p\text{-}p,max}$ that is maybe 50% to 90% of V+.

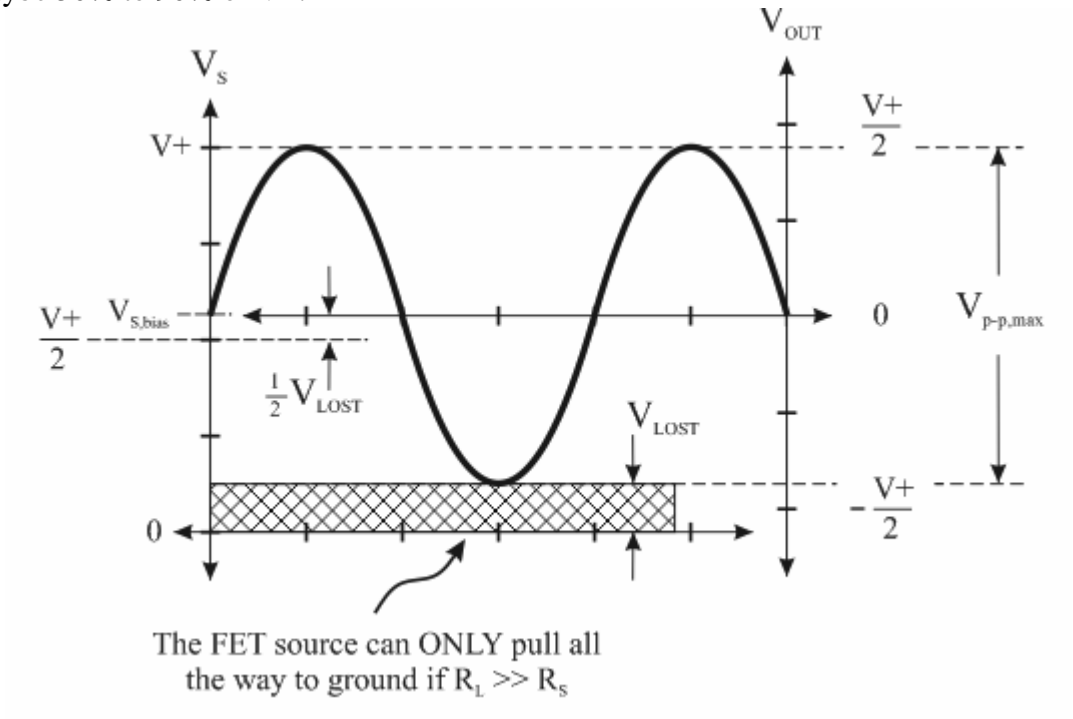

Figure 2 – Maximum Signal Swing at the Source and V_{out}

SOLUTION:

First calculate V_{LOST}:

$$V_{LOST} = V_+ - V_{P-P,\max} \tag{0}$$

Next, look at the situation in figure 3. Figure 3 shows how this circuit behaves and why voltage is lost at the bottom of the signal swing. Imagine that the FET is being driven by a rail-to-rail square wave. At the top of the square wave the left hand side of the output capacitor will be charged to V+ but we also know that the right hand side of the output capacitor C_{out} must be ($V_{p\text{-}p,max}$ / 2). When the sharp falling edge of the square wave turns the FET off then this becomes the same situation as shown in figure 3:

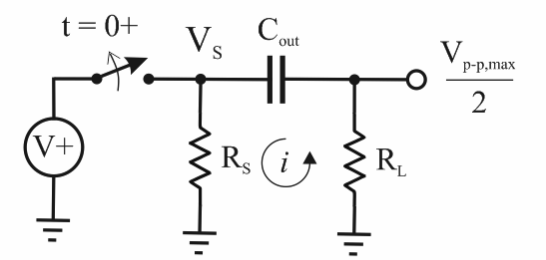

Figure 3 – Situation for a square wave input with a fast falling edge

The voltage across the output capacitor just after the switch turns off at time 0+ is:

$$V_+ - \frac{1}{2}V_{P-P,\max} \tag{1}$$

This voltage establishes a current loop *i* which, in turn, creates a voltage on R_S that is equal to V_{LOST}. As long as C_{out} is large then the lost voltage situation for any waveform will be the same as in this square wave example. This lost voltage is:

$$V_{LOST} = \left(V_+ - \frac{V_{P-P,\max}}{2}\right) \cdot \left(\frac{R_S}{R_S + R_L}\right) \tag{2}$$

All values of this equation are known except R_S so solve the above for R_S to get:

$$R_S = \frac{R_L V_{LOST}}{V_+ - \frac{V_{P-P,\max}}{2} - V_{LOST}} \tag{3}$$

The optimum DC bias voltage at the FET source (from inspection of figure 2) is then:

$$V_{S,bias} = \frac{V_+}{2} + \frac{V_{LOST}}{2} \tag{4}$$

The optimum bias voltage on the gate will be $V_{GS(th)}$ above $V_{S,bias}$. ($V_{GS(th)}$ can be found on the FET datasheet.) Add it to the source voltage to get the desired gate bias voltage:

$$V_{bias} = V_{S,bias} + V_{GS(th)} \tag{5}$$

To set the gate bias voltage, choose a value for R_2 then calculate a value for R_1:

$$R_1 = R_2\left(\frac{V_+ - V_{bias}}{V_{bias}}\right) \tag{6}$$

Finally check the FET DC bias current and power dissipation to make sure these are compatible with the selected FET's absolute maximum limits:

$$i_{S,bias} = \frac{V_{S,bias}}{R_S} \tag{7}$$

Example:

$V+ = 5V$
$R_L = 1k\Omega$
$V_{p\text{-}p,max} = 4V$

The waveform shown in figure 4 is the source voltage for a circuit with poorly optimized bias. In this example, R_S is 1kΩ and the source bias voltage was naively set to 2.5V (half of V+). The circuit is driven with a 4 $V_{P\text{-}P}$ sine wave. If this were a DC couple source follower then this would be a reasonable bias choice but look at the unpleasant result (figure 4) for this circuit when the 1 kΩ load is AC coupled to the source:

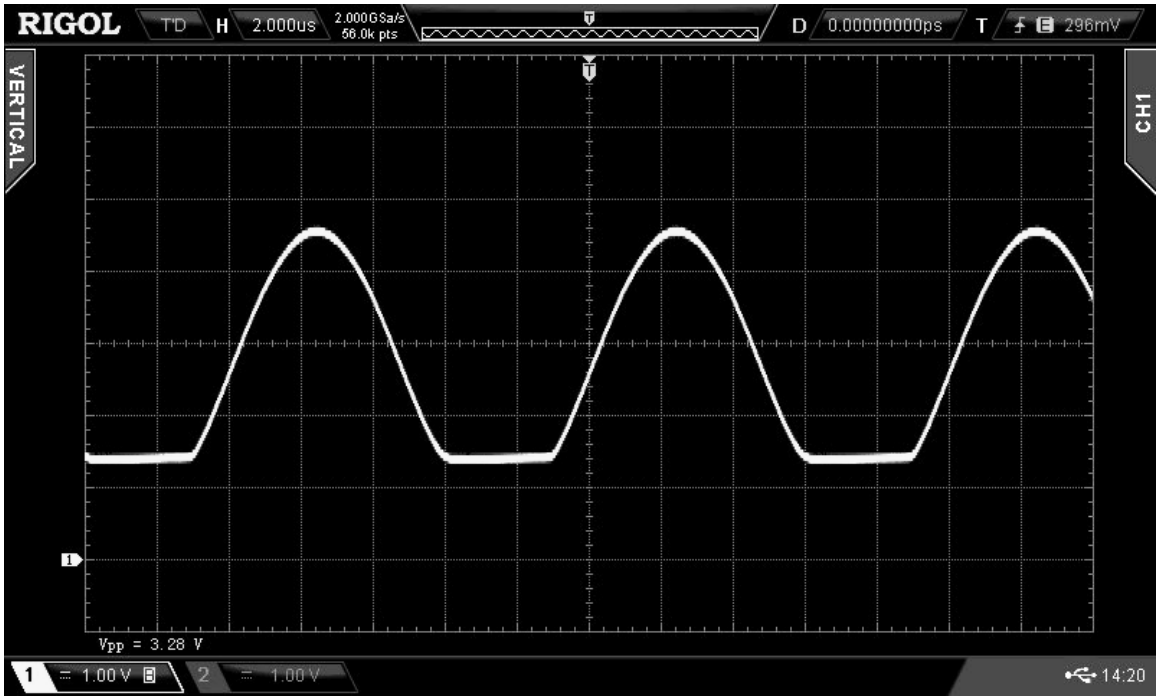

Figure 4 – Source voltage of a poorly optimized circuit

Now let's optimize the bias points for this circuit. First note that because V+ is 5V and $V_{P\text{-}P,max}$ is 4 $V_{P\text{-}P}$ we have therefore chosen V_{LOST} to be 1V. Calculate R_S using equation 3:

$$R_S = \frac{R_L V_{LOST}}{V_+ - \frac{V_{P-P,\max}}{2} - V_{LOST}} \tag{3}$$

$$R_S = \frac{(1k)(1V)}{(5V) - \frac{1}{2}(4V) - (1V)}$$

RS = 500Ω
(use the nearest standard value: 470Ω)

Now calculate the optimum DC bias voltage at the source using equation 4:

$$V_{S,bias} = \frac{V_+}{2} + \frac{V_{LOST}}{2} \tag{4}$$

$$V_{S,bias} = \frac{(5V)}{2} + \frac{(1V)}{2}$$

$$V_{S,bias} = 3V$$

Add the gate-to-source threshold voltage to $V_{S,bias}$ to get V_{bias} (equation 5).
For BSS138 $V_{GS(th)}$ is typically 1.3V:

$$V_{bias} = V_{S,bias} + V_{GS(th)} \tag{5}$$

$$V_{bias} = (3V) + (1.3V)$$

$$V_{bias} = 4.3V$$

At this stage an astute reader might be alarmed that a 4.3V DC gate bias with a 4 V_{P-P} input implies a peak gate voltage that will exceed the (5V) V+ rail. It turns out this is not an issue as long as the maximum gate-to-source voltage limits for the FET are not violated. In fact, we want the maximum gate voltage to rise exactly one $V_{GS(th)}$ above V+. In the case of the BSS138 $V_{GS,max}$ is ±20V so this situation is not a problem.

Now choose $R_2 = 100\ k\Omega$

And find R_1 using equation 6:

$$R_1 = R_2\left(\frac{V_+ - V_{bias}}{V_{bias}}\right) \tag{6}$$

$$R_1 = (100k\Omega)\left(\frac{(5V) - (4.3V)}{(4.3V)}\right)$$

$$R1 = 16.279\ k\Omega$$
(use the nearest standard value: 16.5 kΩ)

Lastly check i_{bias} to make sure it is reasonable for the BSS138:

$$i_{S,bias} = \frac{V_{S,bias}}{R_S} \tag{7}$$

$$i_{S,bias} = \frac{(3V)}{(470\Omega)}$$

$I_{S,bias}$ = 6.4 mA (very reasonable)

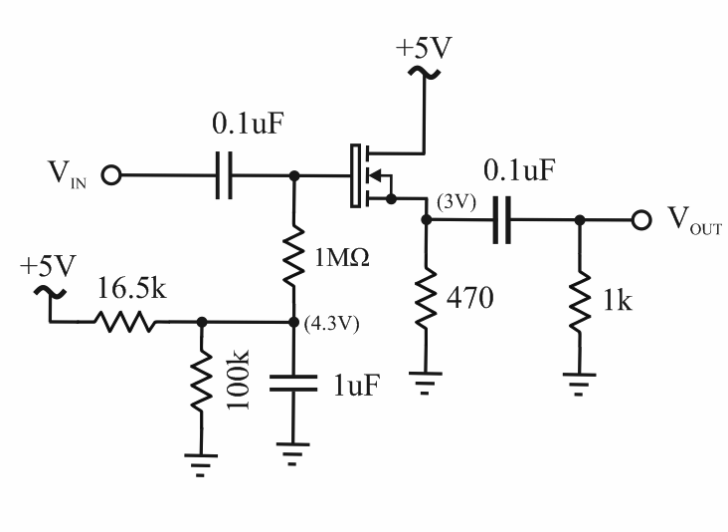

Figure 5 – Circuit with bias point optimized for AC coupled output

Shown here in figure 6 are the results for the now optimized circuit (figure 5). The circuit is driven by a 100 kHz, $4V_{P-P}$ sine wave. Notice that the top and bottom of the sine wave is just starting to clip at the desired $4V_{P-P}$ design limit. Symmetrical clipping of the top and bottom of the wave is a clear sign that this circuit is optimally biased for the best possible peak-to-peak output swing.

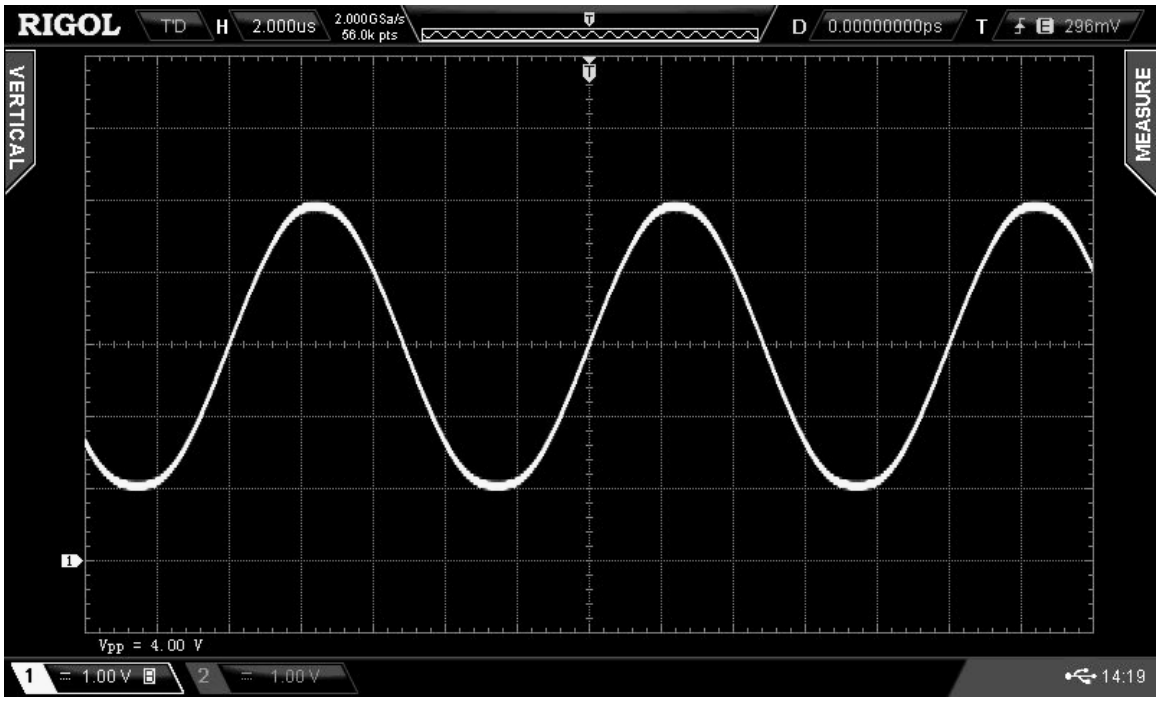

Figure 6 – Source voltage for the well optimized bias point

Conclusion: The source follower is a fabulous circuit for any engineer's tool box. Its characteristics are well documented but beware of biasing pitfalls when AC coupling the output and get the full signal swing you deserve by setting optimum bias points.

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